

**IN THE CLAIMS**

1-64. (canceled)

65. (Currently amended) A CMOS imager comprising:

an array of pixels, disposed on a semiconductor substrate, including a red pixel to provide a red pixel signal to indicate an amount of red light sensed by the red pixel, a green pixel to provide a green pixel signal to indicate an amount of green light sensed by the green pixel, and a blue pixel to provide a blue pixel signal to indicate an amount of blue light sensed by the blue pixel;

an interpolator, disposed on the semiconductor substrate, to receive pixel signals corresponding to groups of pixels of the array, including, for at least one of the groups, a first number of rows of pixels and at least the first number of columns of pixels, and to estimate an amount of green and blue light received by the red pixel using at least the green and blue pixel signals, an amount of red and blue light received by the green pixel using at least the red and blue pixel signals, and an amount of red and green light received by the blue pixel using at least the red and green pixel signals;

at least the first number of analog-to-digital converters, disposed on the semiconductor substrate, coupled to receive pixel signals from the array, to convert the red, green, and blue pixel signals from analog to digital signals, wherein the first number is at least ~~three~~ one;

a register set, disposed on the semiconductor substrate, that is programmable via an external interface, wherein the interpolator is to operate depending on one or more values to be stored in the register set; and

a parallel port interface, external to the imager, to provide output signals associated with the red, green, and blue pixel signals.

66. (previously presented) The CMOS imager of claim 65, wherein the one of the groups is a block of pixels.

67. (previously presented) The CMOS imager of claim 65, further comprising a plurality of conditioning circuits, disposed on the semiconductor substrate, coupled to receive pixel signals from the array, each of the plurality of conditioning circuits corresponding to a respective one of the analog-to-digital converters, wherein the conditioning circuits are to perform correlated double sampling.

68. (previously presented) The CMOS imager of claim 67, wherein the plurality of conditioning circuits includes as many conditioning circuits as there are analog-to-digital converters.

69. (previously presented) The CMOS imager of claim 68, wherein the conditioning circuits are to further perform signal sample and hold.

70. (previously presented) The CMOS imager of claim 68, wherein the conditioning circuits are to further perform gain control.

71. (previously presented) The CMOS imager of claim 67, wherein the conditioning circuits are to further perform gain control.

72. (previously presented) The CMOS imager of claim 67, wherein at least one of the analog-to-digital converters is to process pixel signals of at least two different colors.

73. (previously presented) The CMOS imager of claim 65, wherein at least one of the analog-to-digital converters is to process at least two pixel signals selected from a group

consisting of the red pixel signal, the green pixel signal, and the blue pixel signal.

74. (previously presented) The CMOS imager of claim 65, wherein the interpolator is to perform interpolation in accordance with the one or more values to be stored in the register set.

75. (previously presented) The CMOS imager of claim 74, wherein the interpolator is to weight pixel values in accordance with the one or more values to be stored in the register set.

76. (previously presented) The CMOS imager of claim 65, wherein the parallel port interface is to provide the red, green, and blue pixel signals.

77. (previously presented) The CMOS imager of claim 76, wherein the parallel port interface is to provide the red, green, and blue pixel signals each as eight bit values.

78. (previously presented) The CMOS imager of claim 77, wherein the parallel port interface is to provide the red, green, and blue pixel signals as five, six, and five bit values, respectively.

79. (previously presented) The CMOS imager of claim 65, wherein the parallel port interface is to further provide output signals associated with interpolated signals from the interpolator depending on the one or more values to be stored in the register set.

80. (previously presented) The CMOS imager of claim 65, wherein the groups of pixels comprise only red, green, and blue pixels.

81. (previously presented) A CMOS imager comprising:  
an array of pixels, disposed on a semiconductor substrate, including a red pixel to provide a red pixel signal to indicate

an amount of red light sensed by the red pixel, a green pixel to provide a green pixel signal to indicate an amount of green light sensed by the green pixel, and a blue pixel to provide a blue pixel signal to indicate an amount of blue light sensed by the blue pixel;

an interpolator, disposed on the semiconductor substrate, to receive a group of pixel signals associated with a group of pixels of the array having M rows of pixels and N columns of pixels, the interpolator to estimate an amount of light of first and second colors, received but not sensed by a target pixel, using selected pixel signals within the group of pixel signals associated with pixels that sense light of the first and second colors;

at least M analog processing circuits, disposed on the semiconductor substrate, coupled to receive pixel signals from the array, each of the analog processing circuits comprising respective circuitry to perform correlated double sampling and analog-to-digital conversion, wherein each of the analog processing circuits is coupled to a respective one of at least M signal lines from a column decoder;

a writable and readable register set, disposed on the semiconductor substrate, accessible via an external interface, to store at least one value to affect an output of interpolated pixel signals; and

an external data output port, to provide first output signals associated with the red, green, and blue pixel signals, and, in accordance with the at least one value to be stored in the register set, to further provide second output signals associated with the amount of light of the first and second colors estimated by the interpolator to be received but not sensed by the target pixel.

82. (previously presented) The CMOS imager of claim 81, wherein the group of pixels is a block of pixels.

83. (previously presented) The CMOS imager of claim 81, wherein each of the analog processing circuits further comprises respective circuitry to perform signal sample and hold.

84. (previously presented) The CMOS imager of claim 83, wherein each of the analog processing circuits further comprises respective circuitry to perform signal gain.

85. (previously presented) The CMOS imager of claim 81, wherein the imager comprises an analog processing circuit corresponding with each analog-to-digital converter.

86. (previously presented) The CMOS imager of claim 81, wherein at least one of the analog processing circuits is to process pixel signals of at least two different colors.

87. (previously presented) The CMOS imager of claim 81, wherein the interpolator is to perform interpolation in accordance with the at least one value to be stored in the register set.

88. (previously presented) The CMOS imager of claim 87, wherein the interpolator is to weight pixel values in accordance with the at least one value to be stored in the register set.

89. (previously presented) The CMOS imager of claim 81, wherein the external data output port is to provide the red, green, and blue pixel signals each as eight bit values in parallel.

90. (previously presented) The CMOS imager of claim 89, wherein the external data output port is to further provide the red, green, and blue pixel signals as five, six, and five bit values, respectively.

91. (previously presented) The CMOS imager of claim 81, wherein the external data output port is to provide the second output signals depending on the at least one value to be stored in the register set.

92. (previously presented) The CMOS imager of claim 81, wherein the group of pixels comprises only red, green, and blue pixels.

93. (previously presented) A system comprising:

a writable and readable register set disposed on a semiconductor substrate and coupled via an external input-output port to an external programming interface, the register set storing a value written to the register set via the programming interface;

an array of photodiodes, disposed on the semiconductor substrate, including a first photodiode to provide a first signal to indicate an amount of red light sensed by the first photodiode, and a second photodiode to provide a second signal to indicate an amount of blue light sensed by the second photodiode;

an estimation circuit, disposed on the semiconductor substrate, to receive a group of signals associated with a group of photodiodes of the array and to use the group of signals to estimate an amount of red and blue light received by a pixel having a photodiode configured to sense green light, wherein the group of signals are associated with photodiodes that sense red and blue light, the estimation circuit to provide first and second estimated signals to indicate the amount of the red and blue light, respectively, estimated by the estimation circuit to be received by the pixel; and

an external data output port from which to read out the first output signals associated with the first and second

signals that indicate the amount of red and blue light sensed by the first and second photodiodes, respectively, and, based at least in part on the value stored in the register set, to read out estimated output signals associated with the first and second estimated signals from the estimation circuit.

94. (previously presented) The system of claim 93, wherein the group of photodiodes includes a first number of rows of photodiodes and at least the first number of columns of photodiodes.

95. (previously presented) The system of claim 94, wherein the group of photodiodes is a block of photodiodes.

96. (previously presented) The system of claim 94, further comprising at least the first number of analog processing circuits, disposed on the semiconductor substrate, coupled to receive pixel signals from the array, each of the analog processing circuits comprising respective circuitry to perform correlated double sampling and analog-to-digital conversion.

97. (previously presented) The system of claim 96, wherein each of the analog processing circuits is coupled to a respective one of at least the first number of signal lines from a column decoder disposed on the semiconductor substrate.

98. (previously presented) The system of claim 96, wherein each of the analog processing circuits further comprises respective circuitry to perform signal gain.

99. (previously presented) The system of claim 96, wherein the imager comprises an analog processing circuit corresponding with every analog-to-digital converter.

100. (previously presented) The system of claim 96, wherein at least one of the analog processing circuits is to process pixel signals of at least two different colors.

101. (previously presented) The system of claim 93, wherein the estimation circuit is to estimate in accordance with the value stored in the register set.

102. (previously presented) The system of claim 101, wherein the estimation circuit is to weight values in accordance with the value stored in the register set.

103. (previously presented) The system of claim 93, wherein the estimation circuit is to estimate in accordance with a plurality of values stored in the register set, including the value stored in the register set.

104. (previously presented) The system of claim 103, wherein the estimation circuit is to adjust weighting factors in accordance with the plurality of values stored in the register set.

105. (previously presented) The system of claim 104, wherein the values stored in the register set are the weighting factors.

106. (previously presented) The system of claim 93, wherein the external data output port is to provide the first and estimated output signals as eight bit values in parallel.

107. (previously presented) The system of claim 93, wherein the external data output port is to provide the estimated output signals depending at least on the value stored in the register set.

108. - 123. (Canceled).

124. (previously presented) A method of operating a CMOS imager comprising:

receiving light in an array of pixels, wherein the array of pixels is disposed on a semiconductor substrate, and wherein the array of pixels includes a red pixel to provide a red pixel

signal to indicate an amount of red light sensed by the red pixel, a green pixel to provide a green pixel signal to indicate an amount of green light sensed by the green pixel, and a blue pixel to provide a blue pixel signal to indicate an amount of blue light sensed by the blue pixel;

performing correlated double sampling and analog-to-digital conversion on a group of pixel signals using at least M analog processing circuits, wherein the analog processing circuits are disposed on the semiconductor substrate and coupled to receive pixel signals from the array, and wherein each of the analog processing circuits is coupled to a respective one of at least M signal lines from a column decoder;

providing the group of pixel signals to an interpolator, wherein the interpolator is disposed on the semiconductor substrate, and wherein the group of pixel signals are associated with a group of pixels of the array having M rows of pixels and N columns of pixels,

estimating, using the interpolator, an amount of light of first and second colors, received but not sensed by a target pixel, using selected pixel signals within the group of pixel signals associated with pixels that sense light of the first and second colors;

programming a writable and readable register set to store at least one value to affect an output of interpolated pixel signals, wherein the register set is disposed on the semiconductor substrate and is accessible via an external interface; and

outputting, through an external data output port, first output signals associated with the red, green, and blue pixel signals, and, in accordance with the at least one value to be stored in the register set, second output signals associated

with the amount of light of the first and second colors estimated by the interpolator to be received but not sensed by the target pixel.

125. (previously presented) The method of claim 124, wherein the group of pixels is a block of pixels.

126. (previously presented) The method of claim 124, further comprising performing signal sample and hold using the analog processing circuits.

127. (previously presented) The method of claim 126, further comprising performing signal gain using the analog processing circuits.

128. (previously presented) The method of claim 124, wherein each analog processing circuit corresponds with an analog-to-digital converter.

129. (previously presented) The method of claim 124, further comprising processing pixel signals of at least two different colors using at least one of the analog processing circuits.

130. (previously presented) The method of claim 124, further comprising performing interpolation in accordance with the at least one value to be stored in the register set using the interpolator.

131. (previously presented) The method of claim 130, further comprising weighing pixel values in accordance with the at least one value to be stored in the register set using the interpolator.

132. (previously presented) The method of claim 124, further comprising outputting the red, green, and blue pixel signals each as eight bit values in parallel.

133. (previously presented) The method of claim 124, further comprising outputting the red, green, and blue pixel signals as five, six, and five bit values, respectively.

134. (previously presented) The method of claim 124, further comprising outputting the second output signals depending on the at least one value to be stored in the register set.

135. (previously presented) The method of claim 124, wherein the group of pixels comprises only red, green, and blue pixels.

136. (previously presented) A method of operating a system comprising:

writing a value to a writable and readable register set via an external programming interface, wherein the register set is disposed on a semiconductor substrate and coupled via an external input-output port to the external programming interface;

receiving light in an array of photodiodes, wherein the array of photodiodes is disposed on the semiconductor substrate, and wherein the array of photodiodes includes a first photodiode to provide a first signal to indicate an amount of red light sensed by the first photodiode, and a second photodiode to provide a second signal to indicate an amount of blue light sensed by the second photodiode;

providing a group of signals to an estimation circuit disposed on the semiconductor substrate, wherein the group of signals is associated with a group of photodiodes of the array that sense red and blue light;

estimating, using the estimation circuit and the group of signals, an amount of red and blue light received by a pixel having a photodiode configured to sense green light, and

providing first and second estimated signals to indicate the amount of the red and blue light, respectively, estimated to be received by the pixel; and

outputting, using an external data output port, the first output signals associated with the first and second signals that indicate the amount of red and blue light sensed by the first and second photodiodes, respectively, and, based at least in part on the value stored in the register set, estimated output signals associated with the first and second estimated signals from the estimation circuit.

137. (previously presented) The method of claim 136, wherein the group of photodiodes includes a first number of rows of photodiodes and at least the first number of columns of photodiodes.

138. (previously presented) The method of claim 137, wherein the group of photodiodes is a block of photodiodes.

139. (previously presented) The method of claim 137, further comprising performing correlated double sampling and analog-to-digital conversion using at least the first number of analog processing circuits, wherein the analog processing circuits are disposed on the semiconductor substrate and coupled to receive pixel signals from the array.

140. (previously presented) The method of claim 139, wherein each of the analog processing circuits is coupled to a respective one of at least the first number of signal lines from a column decoder disposed on the semiconductor substrate.

141. (previously presented) The method of claim 139, further comprising performing signal gain using the analog processing circuits.

142. (previously presented) The method of claim 139, wherein each analog processing circuit corresponds with an analog-to-digital converter.

143. (previously presented) The method of claim 139, further comprising processing pixel signals of at least two different colors using at least one of the analog processing circuits.

144. (previously presented) The method of claim 136, wherein the estimation circuit estimates in accordance with the value stored in the register set.

145. (previously presented) The method of claim 144, wherein the estimation circuit weights values in accordance with the value stored in the register set.

146. (previously presented) The method of claim 136, wherein the estimation circuit estimates in accordance with a plurality of values stored in the register set, including the value stored in the register set.

147. (previously presented) The method of claim 146, wherein the estimation circuit adjusts weighting factors in accordance with the plurality of values stored in the register set.

148. (previously presented) The method of claim 147, wherein the values stored in the register set are the weighting factors.

149. (previously presented) The method of claim 136, further comprising outputting the first and estimated output signals as eight bit values in parallel.

150. (previously presented) The method of claim 136, further comprising outputting the estimated output signals depending at least on the value stored in the register set.